InP/InGaAs HBTs Using Crystallographically Defined Emitter Contact Technology

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Abstract — **New self-alignment techniques employing crystallographically defined emitter contact (CDC) technologies have been developed to fabricate InP/InGaAs heterojunction bipolar transistors (HBTs). The CDC technologies utilize the anisotropic wet etching characteristics of the InP and InGaAs dummy emitter layers, grown on the typical HBT layer structure. The shape of the emitter contact is determined by the crystallographically etched profiles of the InP and InGaAs dummy emitter layers. The fabricated HBTs demonstrated excellent device performance characteristics, indicating the effectiveness of the new self-alignment technology.**

I. INTRODUCTION

InP-based heterojunction bipolar transistor (HBT) technology has been rapidly progressing over the past ten years. The current gain cutoff frequency and maximum oscillation frequency have both broken the 300-GHz frequency barrier [1-3]. There are a number of inherent advantages of these devices compared with the more mature GaAs-based HBTs, such as higher operating speed, smaller turn-on voltage, and lower power consumption. These advantages lend themselves well to the development of integrated circuits (IC) characterized by high-speed performance and low power consumption. In addition, InP-based HBT offers material compatibility and integrability with lightwave optical devices such as InP-based photodetectors operating in the wavelength range from 1.3 to 1.55 μm, making it an important technology for long-haul optical communication and signal processing [4].

HBT fabrication technology for IC applications has been developed primarily to reduce extrinsic parasitic-components and to scale down the device's lateral dimensions. To reduce extrinsic device parasitics, the base contacts are made self-aligned to the emitter mesa. Using self-alignment techniques, the emitter and base dimensions can be reduced and thereby minimizing the extrinsic base resistance. A number of different self-alignment techniques have been reported. To avoid excessive undercutting and the resultant large separation between the base contact and emitter mesa in the convention self-alignment technique using wet etching [5], reactive ion etch (RIE) processes can be used, however, which usually result in RIE-induced damage to the etched surface and base layer [6-7]. The approach used in this work is a self-aligned triple mesa process based on the wet etching techniques, which can provide damage-free precise self-alignment.

In this work, new self-alignment techniques are investigated, which are based on two different schemes of CDC technology; one using an InP dummy layer and the other using an InGaAs dummy layer for fabrication of high-frequency InP/InGaAs HBTs.

II. CRYSTALLOGRAPHICALLY DEFINED EMITTER CONTACT TECHNOLOGY

Thereafter, two different schemes of self-alignment using anisotropical etching characteristics of the InP layer and the InGaAs layer are named as "InP CDC technology" and "InGaAs CDC technology", respectively. The device layer structure for InP/InGaAs HBTs employing two CDC technologies are summarized in Table I. The dummy emitter layers were grown on a typical HBT layer structure. A self-aligned contact spacing, which was designed to be 0.14 μm for both CDC technologies, can be adjusted through controlling the thickness of the dummy emitter layers. To obtain the designed spacing, the thickness of the InP dummy emitter layer was designed to be 250 nm in the InP CDC technology. However, the InGaAs dummy emitter layer's thickness was determined to be 530 nm in the InGaAs CDC technology as shown Table I. Due to steeper sidewall angle of InGaAs than that of InP, the InGaAs dummy emitter layer should be thicker than the InP dummy emitter layer to meet the spacing of 0.14 μm. In the InGaAs CDC technology, the two top InGaAs/InP layers are used to transfer an emitter contact pattern to the InGaAs dummy emitter layer in the photolithography process and the heavily-doped (2×10^{19} cm^{-3}) InP emitter layer is employed as an emitter contact layer to obtain a consistent crystallographically defined emitter contact using high etching selectivity between the InGaAs dummy emitter layer and the InP emitter layer [8]. These device structures were grown by chemical beam epitaxy (CBE) and molecular beam epitaxy (MBE) using Si and C for n- and p-type dopants, respectively.

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Table I. Layer structures of InP/InGaAs HBT for (a) InP CDC technology grown by CBE and (b) InGaAs CDC technology grown by MBE.

Layer	Material	Doping (cm^{-3})	Thickness (nm)
Dummy emitter	InP		250
Emitter	n^+-InGaAs	1×10^{19}	100
	n^+-InP	4×10^{19}	50
	n-InP	3×10^{17}	100
Spacer	u-InGaAs	undoped	5
Base	p^+-InGaAs	4×10^{19}	55
Collector	n-InGaAs	4×10^{16}	600
Etch-stop	n-InP	4×10^{16}	10
Subcollector	n^+-InGaAs	1×10^{19}	500

(a)

Layer	Material	Doping (cm^{-3})	Thickness (nm)
Transfer	InGaAs		10
	InP		80
Dummy emitter	InGaAs		530
Emitter	n^+-InP	2×10^{19}	100
	n-InP	4×10^{17}	60
Spacer	u-InGaAs	undoped	5
Base	p^+-InGaAs	4×10^{19}	45
Collector	n-InGaAs	2×10^{16}	600
Etch-stop	n^+-InP	2×10^{19}	10
Subcollector	n^+-InGaAs	2×10^{19}	400

(b)

The new self-alignment technologies utilize the consistent crystallographic wet etching characteristics of InP and InGaAs, respectively. It is well known that chemical wet etching of the InP layer leads to an anisotropic etching profile according to the crystal direction [9]. But, that of InGaAs has been reported to have almost similar properties [10]. The crystallographically etched sidewall, which is configured as a result of selective wet etching of the InP and InGaAs layers in the $[0\,1\,\bar{1}]$ crystal direction, brings about the shape of the emitter contact. Therefore, the emitter fingers are placed parallel to the $[0\,1\,\bar{1}]$ crystal direction to obtain the shape of the crystallographically defined emitter contact. The fabrication sequence of each CDC technology is described schematically in Fig. 1. Two CDC technologies consist of four fabrication steps, including (1) wet etching of dummy emitter, (2) emitter metallization, (3) wet etching of remaining dummy emitter, and (4) emitter mesa and base metallization, as shown in Fig. 1. The InP and InGaAs layers are etched using HCl-based etchant (HCl:H3PO4) and H_3PO_4-based etchant (H_3PO_4:H_2O_2:H_2O), respectively. The subsequent device fabrication steps are the same as those in the previous work [11]. Fig. 2 shows the scanning electron micrograph (SEM) photographs of the emitter contacts employing two CDC technologies, demonstrating that new self-alignment techniques are very effective in producing the consistent self-alignment of the emitter and base contacts. But, InGaAs CDC technology provides more reproducible self-alignment than InP CDC technology due to more precise and consistent undercut profile as shown in Fig. 2.

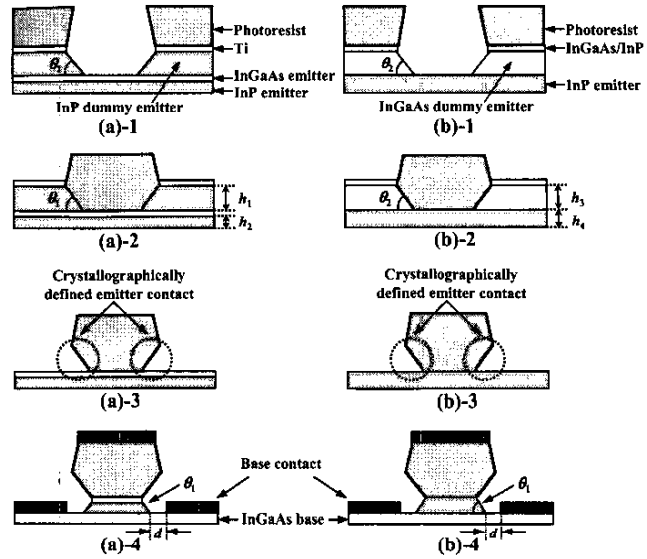
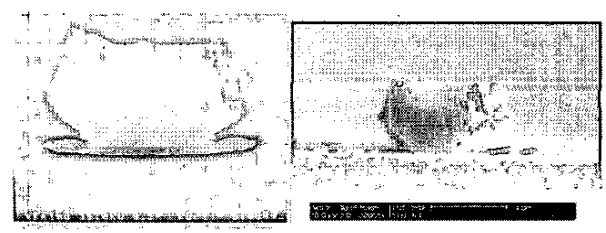


Fig. 1. Fabrication steps of (a) InP CDC technology and (b) InGaAs CDC technology: (1) wet etching of dummy emitter, (2) emitter metallization, (3) wet etching of remaining dummy emitter, and (4) emitter mesa and base metallization (cross section of an emitter aligned parallel to the $[0\,1\,\bar{1}]$ crystal direction).



(a) (b)

Fig. 2. SEM photographs of the emitters contacts using (a) InP CDC technology and (b) InGaAs CDC technology.

In Fig. 1, the spacing (d) between the emitter mesa and the base contact is approximately defined as

$$d \cong \frac{h_1}{\tan\theta_1} - \frac{h_2}{\tan\theta_1} \quad (1)$$

$$d \cong \frac{h_3}{\tan\theta_2} - \frac{h_4}{\tan\theta_1} \quad (2)$$

where h_1 and h_2 are the thickness of the InP dummy emitter layer and the InP emitter layer and θ_1 is the etch-revealed InP sidewall angle in Equation (1), corresponding to the InP CDC technology, while h_3 and h_4 are the thickness of the InGaAs dummy emitter layer and the InP emitter layer

and θ_2 is the InGaAs sidewall angle in Equation (2), corresponding to the InGaAs CDC technology. According to the experimental results reported by Huang *et al.* [12], there exists an optimum spacing in the self-aligned devices to obtain simultaneously the best DC and RF performances. In the two CDC technology, the optimum spacing (d) can be easily designed only by adjusting thickness of the layers because the values of θ_1 and θ_2 are fixed to be 35° and 55° due to the crystallographical etching characteristics of these layers [9-10].

III. Results and Discussion

To investigate the effects of the two CDC technologies on device's performance, DC and RF measurements are performed. The common-emitter I_C-V_{CE} characteristics of the fabricated 1×20 μm^2 devices are shown in Fig. 3. The offset voltage was measured to be as low as 70 mV. The knee voltages of the devices were approximately 0.5 V up to a collector current density (J_C) of 1×10^5 A/cm^2 and the collector-emitter breakdown voltages (BV_{CEO}) were as high as 8.9 V. From Gummel plots, the ideality factors for the collector (n_C) and base (n_B) currents were found to be 1.01 and 1.28, respectively. From the upward I_C-V_{CE} curves at high collector current in Fig. 3 (a), one can infer that relatively high doping of the InGaAs collector layer in the InP CDC technology causes rather poor output conductance properties than those of the devices using InGaAs CDC technology.

Devices with various emitter sizes were fabricated to investigate the emitter size effect. The performance was characterized by investigating inverse current gain ($1/h_{FE}$) versus the perimeter (L_E) to area (S_E) ratio of emitters [13]. This relationship can be expressed as

$$\frac{1}{h_{FE}} = \frac{1}{h_{FE,0}} + \frac{J_{B,P}}{J_C} \times \frac{L_E}{S_E} \qquad (3)$$

where $h_{FE,0}$ is the intrinsic bulk current gain and $J_{B,P}$ is the base surface recombination current density. Fig. 4 shows the dependence of $1/h_{FE}$ on perimeter to area ratio (L_E/S_E) for the fabricated InP/InGaAs HBTs using InP CDC technology. From the slope of the solid line shown in Fig. 4, $J_{B,P}$ was estimated to be 0.74×10^{-6} A/μm at J_C = 4 × 10^4 A/cm^2. Compared to more mature InGaP/GaAs HBT technology with a value of 1.8×10^{-6} A/μm [13], lower base surface recombination current density ($J_{B,P}$) was obtained. This result indicates that the inherent low surface recombination velocities of InP/InGaAs materials as well as the damage-free CDC technology substantially suppress the degradation of current gain for small-size devices. Therefore, the new self-alignment technologies are very effective in preserving high current gain of the device even down to submicron emitter dimensions.

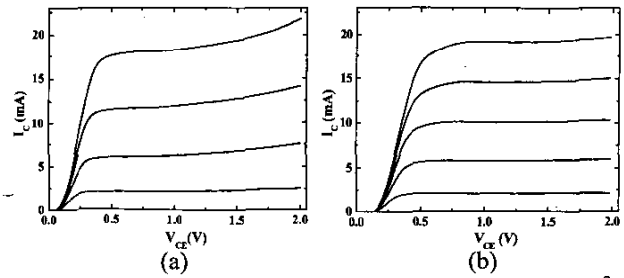


Fig. 3. Common-emitter I_C-V_{CE} characteristics of 1×20 μm^2 InP/InGaAs HBTs employing (a) InP CDC technology and (b) InGaAs CDC technology.

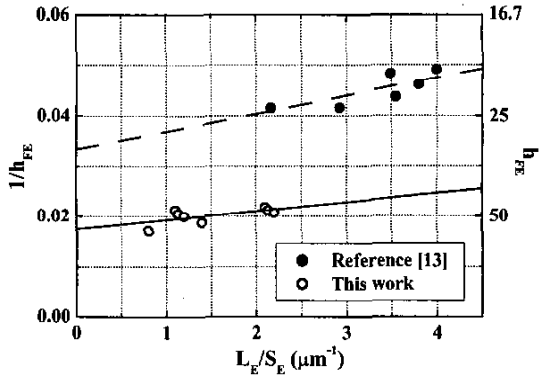
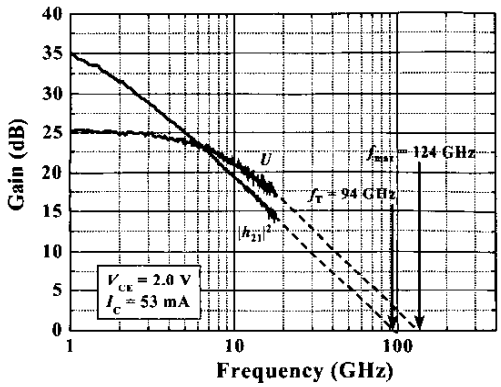


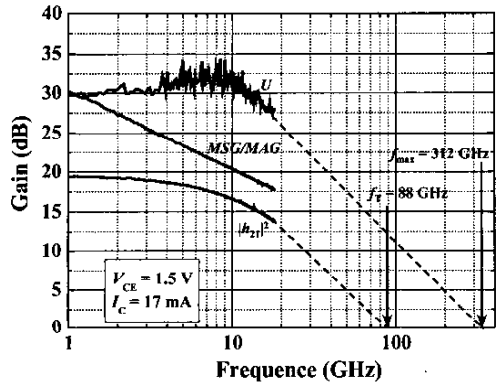
Fig. 4. Dependence of inverse current gain ($1/h_{FE}$) on perimeter to area ratio (L_E/S_E) for fabricated devices using InP CDC technology at a collector current density of J_C = 4×10^4 A/cm^2.

Microwave S-parameter measurements were performed on wafer. Fig. 5 shows the frequency dependency of the current gain ($|h_{21}|^2$), the maximum stable gain/maximum available gain (MSG/MAG), and the unilateral power gain (U), obtained from the fabricated HBTs with an emitter size of 1 × 20 μm^2. The current gain cutoff frequency (f_T) of 94 GHz and maximum oscillation frequency (f_{max}) of 124 GHz in the device employing the InP CDC technology were estimated by extrapolating the measured $|h_{21}|^2$ and U with a 20 dB/decade falloff slope in Fig 5 (a). From the results of small-signal parameter extraction and optimization based on T-equivalent-circuit model, the extracted base-collector capacitance (C_{BC}) is estimated to be 40 fF. Rather large C_{BC} is attributed to the base mesa process that is not optimized for high-speed operation, resulting in a considerable extrinsic parasitic-component. Also, the peaks of f_T and f_{max} were obtained at a collector current density of J_C = 2.5 × 10^5 A/cm^2. These results indicate that the frequency peak values were shifted to higher collector current density due to relatively high n-type doping in the collector layer. In the case of the InGaAs CDC technology, the maximum f_T and f_{max} were 88

and 312 GHz, respectively. The peaks of f_T and f_{max} were measured at lower collector current density ($J_C = 8\times10^4$ A/cm^2) because of lower collector doping level. High frequency performances of $f_{max} > 300$ GHz were observed due to the very low product of reduced R_B and C_{BC}, resulting from the InGaAs CDC technology.



(a)



(b)

Fig. 5. Dependence of $|h_{21}|^2$, *MSG/MAG*, and U on the fabricated HBTs with a 1×20 μm^2 emitter size: (a) InP CDC technology and (b) InGaAs CDC technology.

IV. Conclusion

New self-alignment technologies employing the two CDC technologies are successfully developed for high-speed InP/InGaAs HBTs. The two CDC technologies utilize the anisotropic wet etching characteristics of InP and InGaAs, respectively. The fabricated InP/InGaAs HBTs with a 1 × 20 μm^2 emitter area exhibited frequency performances of f_T = 94 GHz and f_{max} = 124 GHz in the InP CDC technology and f_T = 88 GHz and f_{max} = 312 GHz in the InGaAs CDC technology, respectively. The good overall performance of the fabricated HBTs demonstrates the effectiveness of the new CDC technologies, characterized by reproducible self-alignment of the emitter and base contacts with the damage-free etched surface. Newly developed CDC technology is promising for fabricating the sub-micron dimension InP/InGaAs HBT and obtaining high-speed performance characteristics for IC applications.

References

[1] J. I. Song, K. B. Chough, C. J. Palmstrom, B. P. V. D. Gaag, and W.-P. Hong, "Carbon-doped based InP/InGaAs HBTs with f_{max} = 200 GHz," *IEEE Device Research Conf., 1994*, paper IVB-5.

[2] M. W. Dvorak, C. R. Bolognesi, O. J. Pitts, and S. P. Watkins, "300 GHz InP/GaAsSb/InP double HBTs with high current capability and $BV_{CEO} \geq 6$ V," *IEEE Electron Device Lett.*, vol. 22, no. 8, pp. 361-363, 2001.

[3] M. Rodwell, Y. Betser, S. Jaganathan, T. Mathew, P. Sundararajan, S. C. Martin, R. P. Smith, Y. Wei, M. Urteaga, D. Scott, and S. Long, "Submicron lateral scaling of HBTs and other vertical-transport devices: towards THz bandwidths," *2000 GAAS*, pp. 1-4, 2000.

[4] K. Yang, A. L. Gutierrrez-Aitken, X. Zhang, G. I. Haddad, and P. Bhattacharya, "Design, modeling, and characterization of monolithically integrated InP-based (1.55 μm) high-speed (24 Gb/s) p-i-n/HBT front-end photoreceivers", *IEEE J. Lightwave Technol.*, vol. 14, pp. 1831-1839, 1996.

[5] Y. Matsuoka, S. Yamahata, and T. Ishibashi, "High-efficiency operation of AlGaAs/GaAs power heterojunction bipolar transistors at low collector supply voltage," *Electron. Lett.*, vol. 27, pp. 982-984, 1993.

[6] H. Masuda, T. Tanoue, T. Oka, A. Terano, M. W. Pierce, K. Hosomi, K. Ouchi, and T. Mozume, "Novel self-aligned sub-micron emitter InP/InGaAs HBT's using T-shaped emitter electrode," *1995 IEEE Proceeding of Indium Phosphide and Related Materials*, pp. 644-647, May 1995.

[7] M. Hafizi, "Submicron, fully self-aligned HBT with an emitter geometry of 0.3 μm," *IEEE Electron Device Lett.*, vol. 18, no. 7, pp. 358-360, July 1997.

[8] M. T. Fresina, S. L. Jackson, and G. E. Stillman, "InP/InGaAs HBTs with n^+-InP contacting layers grown by MOMBE using $SiBr_4$," *Electron. Lett.*, vol. 30, pp. 2177-2178, 1994.

[9] S. Adachi and H. Kawaguchi, "Chemical etching characteristics of (001) InP," *J. Electrochem. Soc.*, vol. 128, no. 6, pp. 1342-1349, June 1981.

[10] A. Stano, "Chemical etching characteristics of InGaAs/InP and InAlAs/InP heterostructures," *J. Electrochem. Soc.*, vol. 134, no. 2, pp. 448-452, February 1987.

[11] M. Kim, T. Kim, S. Jeon, M. Yoon, Y. S. Kwon, and K. Yang, " Performance of new self-aligned InP/InGaAs HBT's using crystallographically - defined emitter contact technology," *2001 IEEE Proceeding of Indium Phosphide and Related Materials*, pp. 220-223, May 2001.

[12] C. E. Huang, C. P. Lee, H. C. Liang, and R. T. Huang, "Critical spacing between emitter and base in InGaP heterojunction bipolar transistors (HBTs)," *IEEE Electron Device Lett.*, vol. 23, no. 10, pp. 576-578, October 2002.

[13] T. Oka, K. Hirata, K. Ouchi, H. Uchiyama, K. Mochizuki, and T. Nakamura, "Small-scaled InGaP/GaAs HBT's with WSi/Ti base electrode and buried SiO_2," *IEEE Trans. Electron Devices*, vol. 45, no. 11, pp. 2276-2282, 1998.